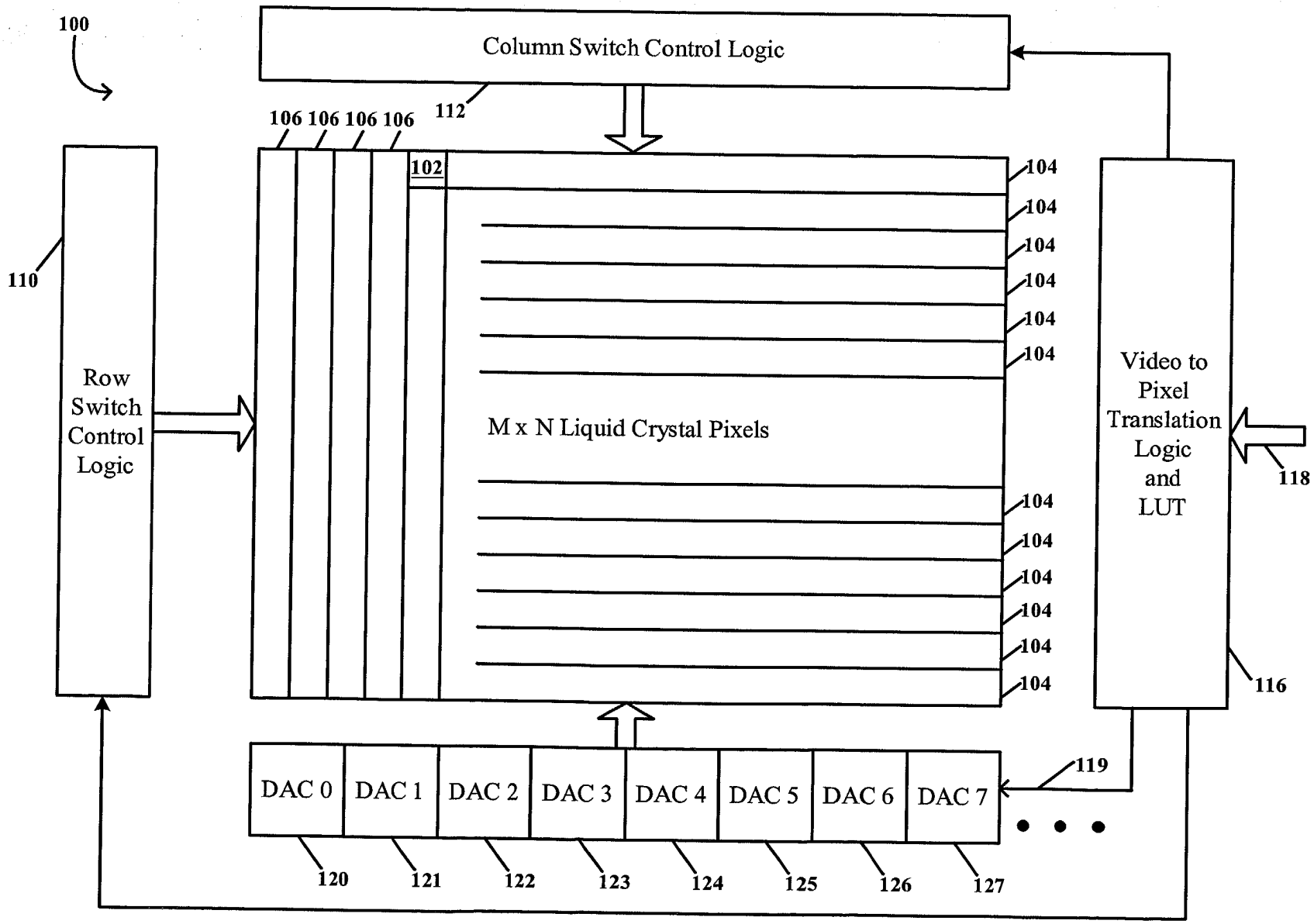
100
Column Switch Control Logic
112
106 106 106 106
102
104
104
104
104
104
104
110
Row Switch Control Logic
M x N Liquid Crystal Pixels
Video to Pixel Translation Logic and LUT
118
104
104
104
104
104
104
116
119
DAC 0
DAC 1
DAC 2
DAC 3
DAC 4
DAC 5
DAC 6
DAC 7
120
121
122
123
124
125
126
127

FIGURE 1

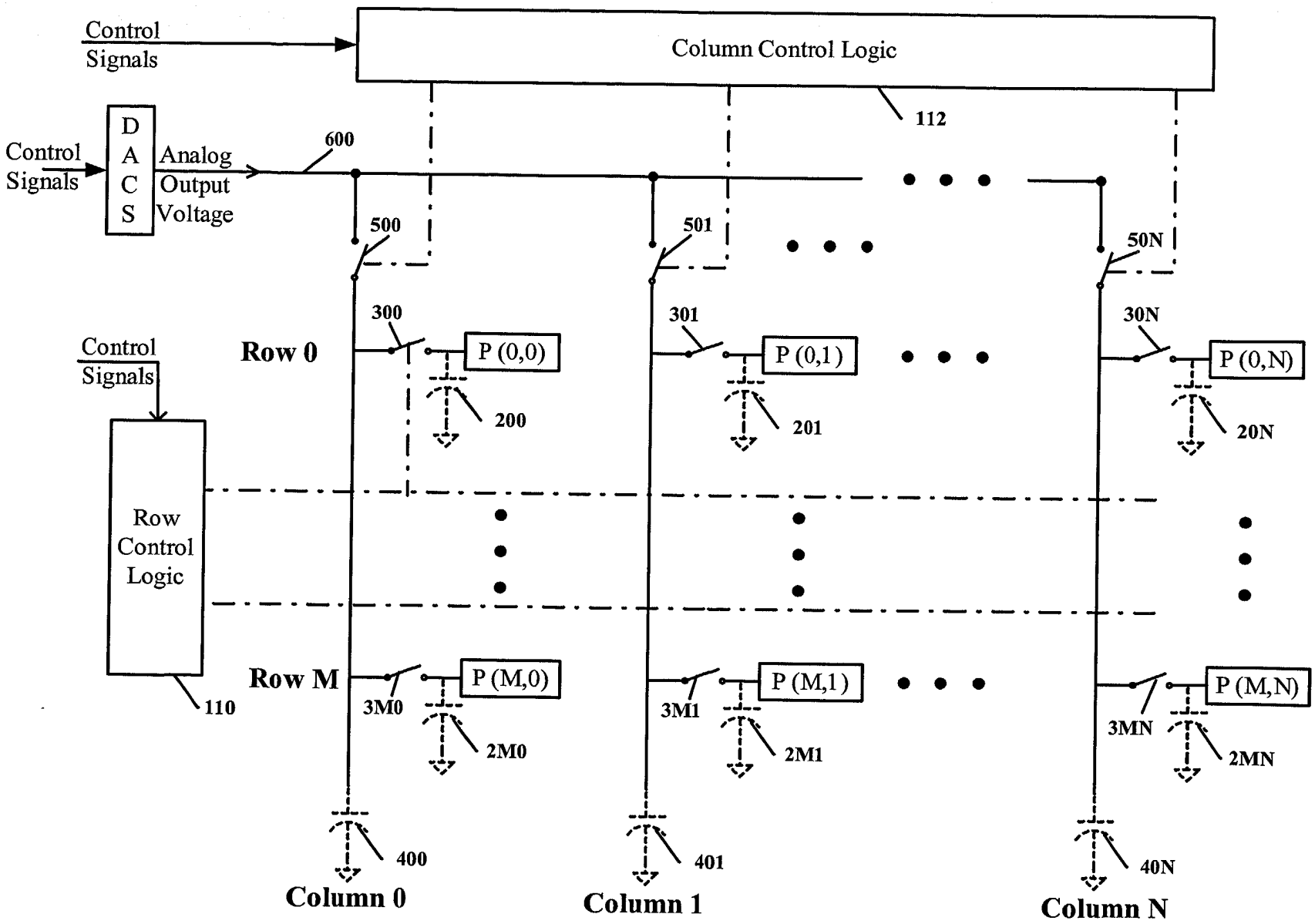

FIGURE 2

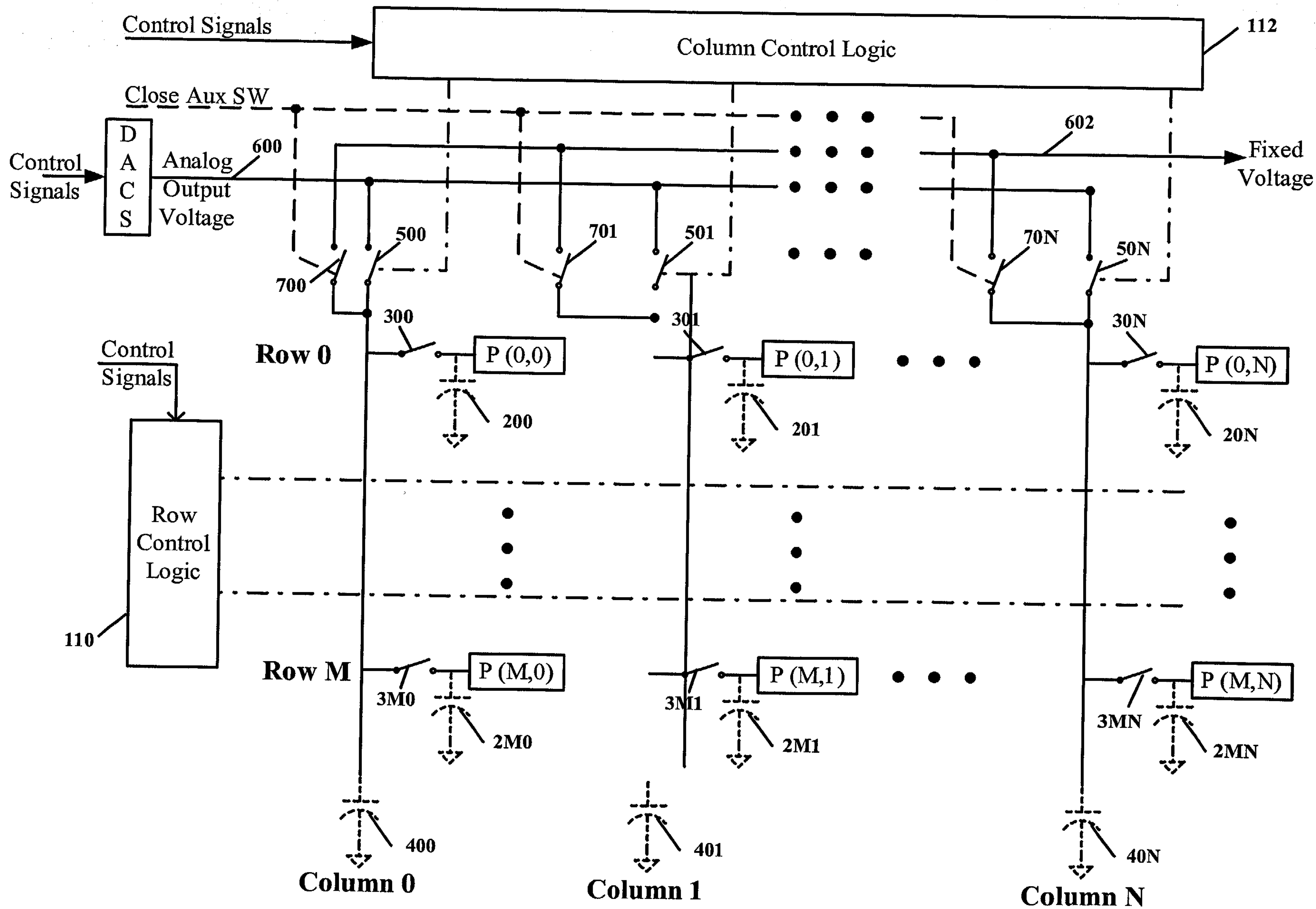
Control Signals
Column Control Logic
112
Close Aux SW
Control Signals
D A C S
Analog Output Voltage
600
602
Fixed Voltage
700
500
701
501
70N
50N
300
301
30N
Row 0
P (0,0)
P (0,1)
P (0,N)
200
201
20N
Control Signals
Row Control Logic
110
Row M
P (M,0)
P (M,1)
P (M,N)
3M0
3M1
3MN
2M0
2M1
2MN
400
401
40N
Column 0
Column 1
Column N

FIGURE 3

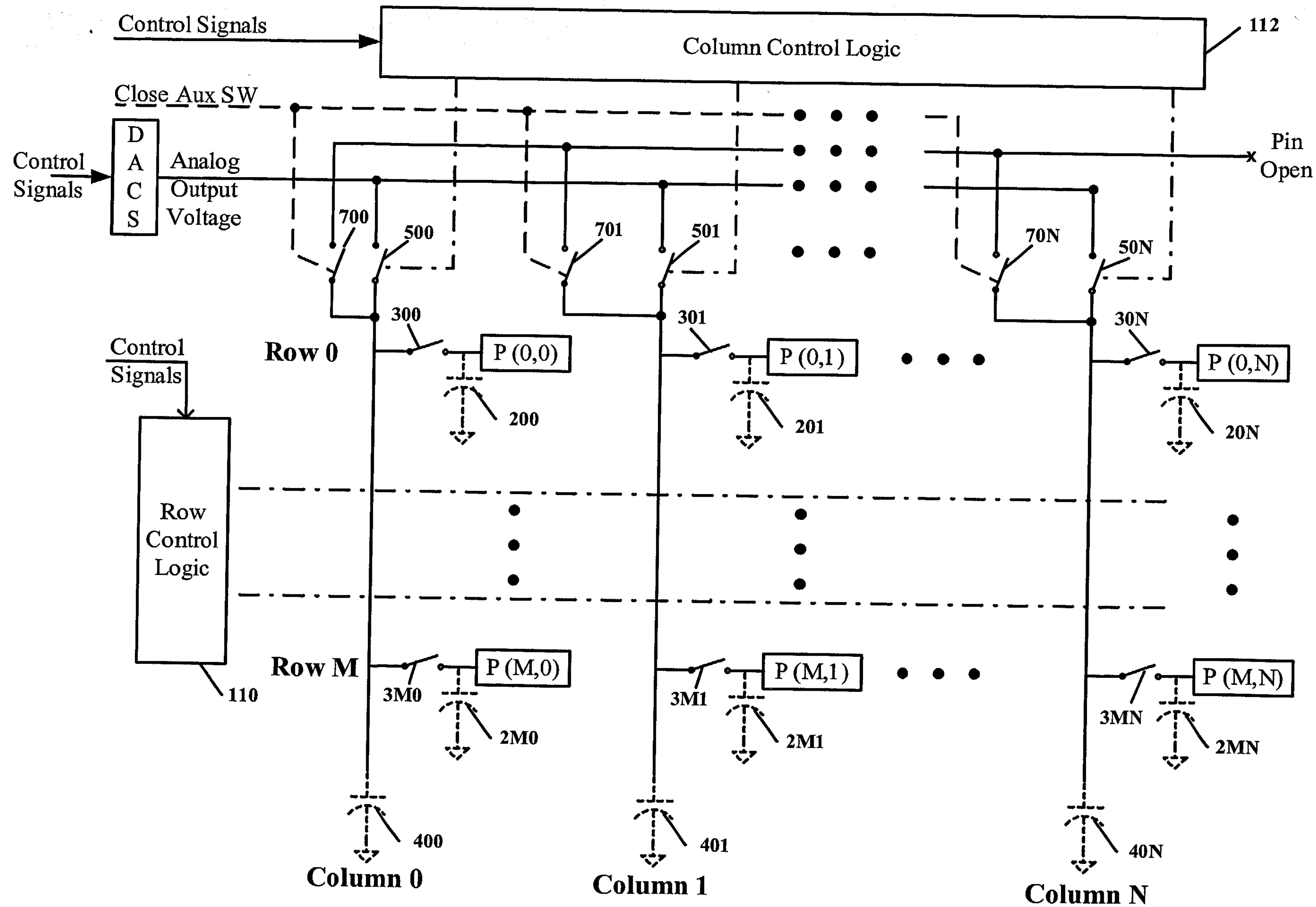
Control Signals
Column Control Logic
112
Close Aux SW
Control Signals
D A C S
Analog Output Voltage
Pin Open
700
500
701
501
70N
50N
300
301
30N
Row 0
P (0,0)
P (0,1)
P (0,N)
200
201
20N
Control Signals
Row Control Logic
110
Row M
P (M,0)
P (M,1)
P (M,N)
3M0
3M1
3MN
2M0
2M1
2MN
400
401
40N
Column 0
Column 1
Column N

FIGURE 4

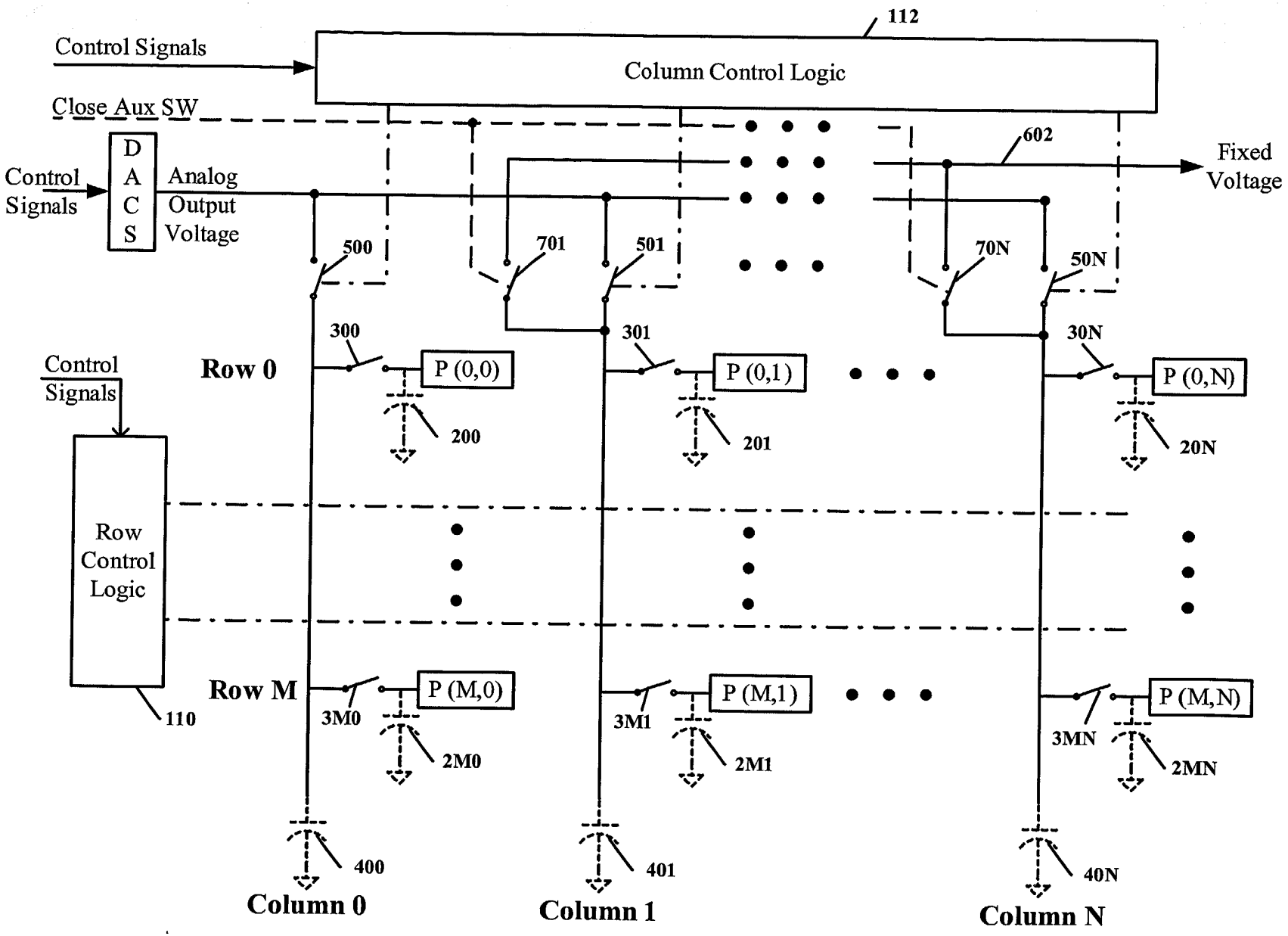

FIGURE 5

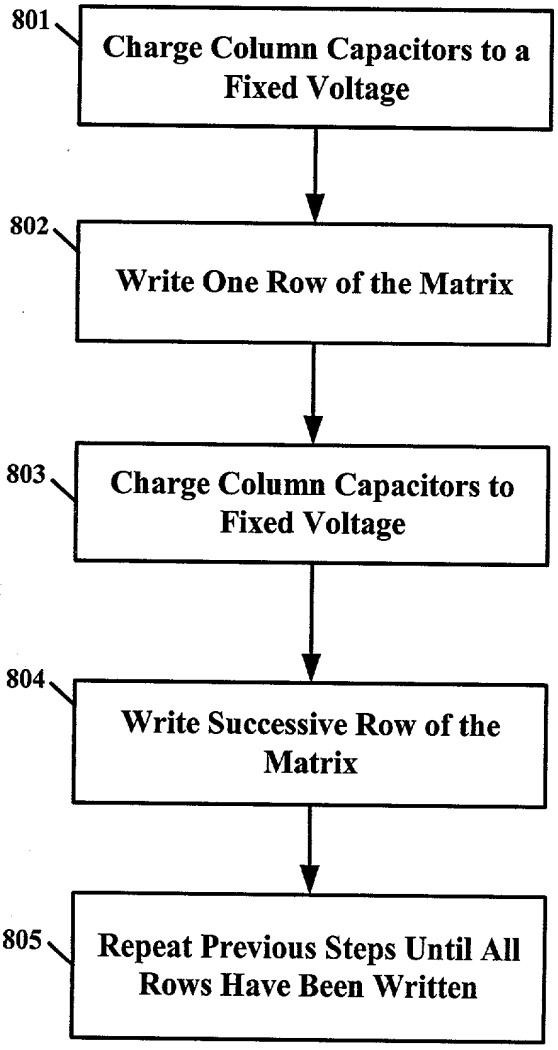

FIGURE 6

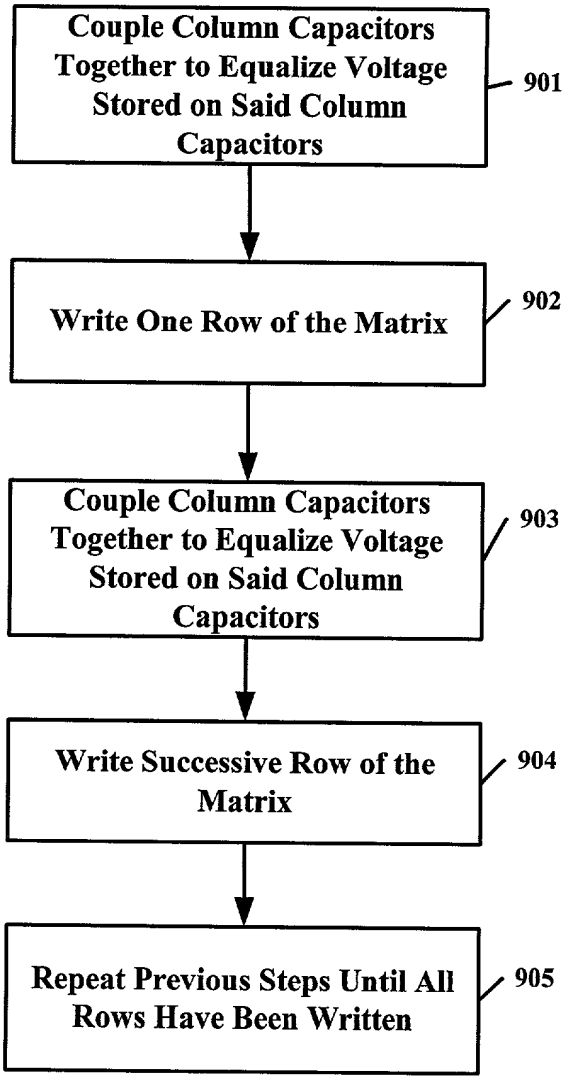

FIGURE 7

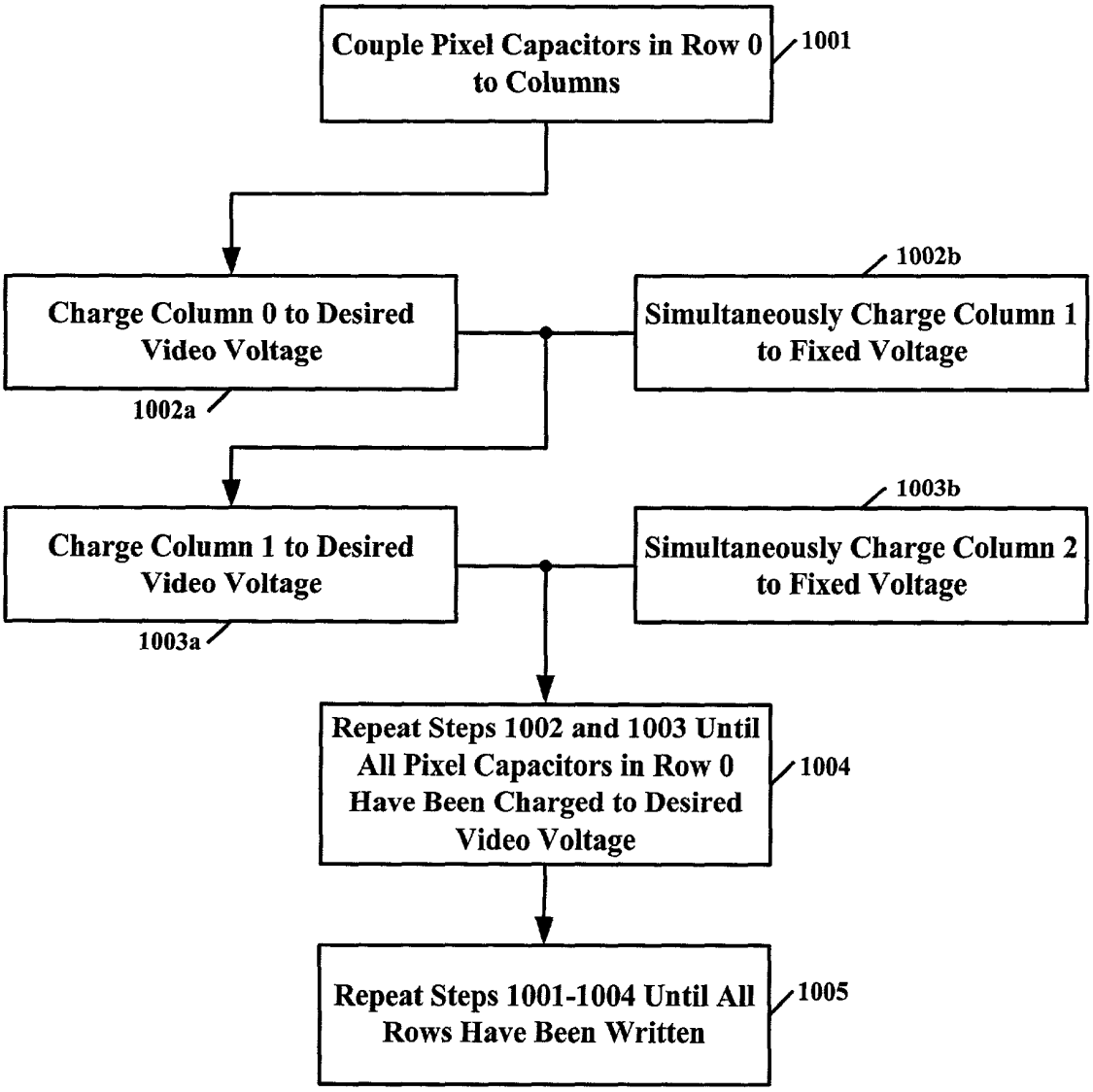
Couple Pixel Capacitors in Row 0 to Columns
1001
Charge Column 0 to Desired Video Voltage
1002a
1002b
Simultaneously Charge Column 1 to Fixed Voltage
Charge Column 1 to Desired Video Voltage
1003a
1003b
Simultaneously Charge Column 2 to Fixed Voltage
Repeat Steps 1002 and 1003 Until All Pixel Capacitors in Row 0 Have Been Charged to Desired Video Voltage
1004
Repeat Steps 1001-1004 Until All Rows Have Been Written
1005

FIGURE 8